Docket No.: EN9-99-026
(PATENT)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:
Douglas O. Powell et al.

Application No.: 09/665,366 Art Unit: 3726

Filed: September 19, 2000 Examiner: Compton, Eric B.

For: ORGANIC DIELECTRIC ELECTRONIC INTERCONNECT STRUCTURES AND METHOD FOR MAKING

DECLARATION UNDER 37 CFR § 1.131

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

I, Douglas O. Powell, a co-inventor of the invention defined in U.S. patent application 09/665,336 hereby declare that:

I have reviewed and understand the contents of the Final Office Action dated 05/10/2004.

I understand that the Examiner has rejected the claims in this application under 35 U.S.C. § 103(a) as being obvious over various combinations of cited art. Specifically:

Claims 1-3, 7-10, 12-14, 16-18, 20-21, 37-42, 45-48, 51-53, 64-68, and 79-80 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Takenouchi (5,744,758) in view of McCormack (6,054,761).

Claims 4-6, 11, 15, 19, 24-33, 35-36, 49-50, and 60-63 were rejected under 35 U.S.C. § 103 (a) as being unpatentable over Takenouchi/McCormack in view of Lake (4,915,983).

Claims 22-23 were rejected under 35 U.S.C. § 103 (a) as being unpatentable over Takenouchi/McCormack in view of Arndt (3,601,523).

Claims 34 and 59 were rejected under 35 U.S.C. § 103 (a) as being unpatentable over Takenouchi/McCormack in view of Dishon (4,921,157).

Claims 37-44 and 69-78 were rejected under 35 U.S.C. § 103 (a) as being unpatentable over Takenouchi/McCormack in view of Pepe (5,635,010).

Each rejection was made over a combination of art that included McCormack (6,054,761) (McCormack).

McCormack was filed December 1, 1998.

I declare that, prior to the McCormack filing date, I had conceived the present invention and had prepared drawings and or other descriptions of the invention that were sufficiently specific to enable a person of skill in the art to practice the invention.

A copy of Invention Disclosure END8-1998-0164 is attached to this Declaration as corroborating evidence. The attached is a true copy with only the dates redacted. Each redacted date is prior to the filing date of McCormack. The attached disclosure is sufficiently specific that a person of skill in the art, once in possession of the disclosure, could have practiced the invention.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements are made with the knowledge that willful false statements and the like so made are punishable by fine, or imprisonment, or both under 18 U. S. C. § 1001 and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Douglas O. Powell Douglas O. Powell, Date 8/31/2004.

-to JRS/SLC

Organic Dielectric Electronic Interconnect Structures and Method for Making

Atty. Work Copy

Disclosure END8-1998-0164

Created By: Douglas Powell **Created On:**
Last Modified By: Douglas Powell **Last Modified On:**

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Required fields are marked with the asterisk (*) and must be filled in to complete the form.

Summary

Status	Under Evaluation
Processing Location	END
Functional Area	MD-(KULLE/LEVINE) Central Engineering
Attorney/Patent Professional	Ronald Kaschak/Endicott/IBM
IDT Team	John Slack/Endicott/IBM
Submitted Date	
Owning Division	MD
PVT Score	To calculate a PVT score, use the 'Calculate PVT' button.

Inventors with Lotus Notes ID's
Inventors: Douglas Powell/Endicott/IBM

Inventor Name > denotes primary contact	Inventor Serial	Div/Dept	Manager Serial	Manager Name
Powell, D.O. (Douglas)	074991	29/T23G	210030	Markovich, V. (Voya)

Inventors without Lotus Notes ID's

IDT Selection K. Papathomas & T. Horn - out.

IDT Team:	Attorney/Patent Professional:
John Slack/Endicott/IBM	Ronald Kaschak/Endicott/IBM

Response Due to IP&L :

Main Idea

***Title of disclosure (In English)**
Organic Dielectric Electronic Interconnect Structures and Method for Making

***Idea of disclosure**

1. Describe your invention, stating the problem solved (if appropriate), and indicating the advantages of using the invention.
Provides for multi-layer electronic interconnect structures, with organic dielectrics, which are fabricated with a parallel layer joining process. These structures do not require plated through holes (PTH's) in order to make interconnections between circuit features on different layers. Traditional multi-layer printed wiring boards (PWB's) use PTH's to interconnect the various circuit layers. The disadvantage of PTH's is the area excluded from use for interconnect wiring by the holes, including the tolerance circle determined by the uncertainty of the hole locations relative to the circuitry. As circuit density increases, and feature size decreases, the area fraction excluded by PTH's increases, since it has not been

possible to scale the exclusion circle proportionately with other circuit features. This effect limits the achievable increases in circuit density. Sequential build-up (SBU) micro-via technologies (e.g. Surface Laminar Circuit - SLC) reduce, or even eliminate, the need for PTH's for interlayer connections, thus allowing higher interconnect densities than PTH's. However, the sequential nature of the process has the following major disadvantages:

1. Cumulative yield loss for each additional layer added to the previous layer structure.
2. Long cycle times, since layers are added in sequence.

The parallel joining process and structures provided by this invention eliminate these two problems. Additionally, the process consists of relatively few and simple process steps, using no high cost materials. This leads to higher yields and lower costs. The disclosed structures are an organic analog to multi-layer ceramic (MLC) structures.

These multi-layer, organic dielectric, electronic interconnect structures can be used for the following types of applications:

1. Integrated circuit package substrates (chip carriers). The driver here is to provide the electrical advantages of organic vs ceramic dielectrics, while providing interconnect density equivalent to or higher than MLC substrates, at a lower cost than other organic alternatives.
2. PWB's for mounting and interconnecting the wide array of components that make up electronic products. Especially useful for products requiring the highest levels of interconnect density or miniaturization (minimization of weight or volume).
3. High density interconnect "patches" or appliqués, which can be joined to lower density interconnect structures (e.g. traditional PWB's) using the same joining methods employed in fabricating the multi-layer patch. This provides for a localized area of high density interconnect where needed, without forcing the entire structure to be built at the premium costs required for the high density area.

2. How does the invention solve the problem or achieve an advantage,(a description of "the invention", including figures inline as appropriate)?

1. Individual layers of conductive circuitry are patterned on a dielectric sheet or film, with the dielectric layer having holes completely filled with conductive material at all locations where it is desired to make electrical connection to circuitry on another layer which will be on the opposite side of the dielectric layer from the current conductive circuit pattern. A thin layer of a low melting metal or metal alloy (solder) is deposited either on the exposed surface of the conductive hole fill material on the side opposite of the circuit pattern (preferred), or on the exposed surface of the circuit pattern directly above/below the conductively filled hole, with a size approximately the same as the hole aperture. The exposed surface of the conductive hole fill material must be solderable with the solder composition chosen, and the solder metal chosen must be capable of soldering to the exposed surface of the conductive circuitry. The solder must contain tin, or another metal which can be soldered, without flux, after pretreatment with a fluorine containing plasma. Figure 8 is a schematic cross section of a portion of a layer at this point in the process.

2. Layers from step 1 are subjected to a fluorine containing plasma in accordance with US 4,921,157, 5,407,121 and/or 5,776,551. This step allows low temperature solder joining (less than 240°C) without using a flux. In this fashion, there are no flux residues after joining which could lead to reliability problems.

3. The various layers for a particular final interconnect structure are stacked up in sequence, with each layer aligned and registered to the preceding layer, such that the conductively filled holes on one layer overlap the circuitry features on the adjacent layer to which they are to be joined. After alignment, the stack of layers is heated to a temperature sufficient to allow the solder to melt, wet and join the conductive hole plugs on each layer to the circuitry on the adjacent layers, and then

cooled to allow further processing. Figure 10 is a schematic cross section of a portion of an interconnect structure after joining.

4. The joined structure is placed in a vacuum chamber, and a low viscosity, thermosetting resin is gated into one or more edges of the joined structure. The resin is allowed to flow throughout the gaps between the layers driven by capillary forces and the atmospheric pressure behind the resin supply. After all the void space in the structure has been fully infused with the liquid resin, the structure is heated to a temperature and for a time adequate to cure the liquid resin to a solid state. Figure 11 is a schematic cross section of a portion of an interconnect structure after resin infusion and cure.

The interconnect structure may be complete at this time, or optionally, it may be drilled, plated and circuitized (using standard PWB processes) to allow mounting of pin-in-hole components, mounting holes may be drilled, it may be used as a core/subcomposite in a higher level laminated interconnect structure, etc.

The finishing operations are similar to those for traditional PWB's: application of a solder mask, modifying the surface finish (organic solder preservative, Ni/Au plating, solder coating, etc.), testing, machining to final outline, etc. Any of these finishing operations can be applied as needed, with the same wide variety of sequences as applicable to ordinary PWB's.

A more detailed description of exemplary processes follows.

Starting Material: Starting material is a dielectric sheet or film with a continuous conductive layer on at least one surface. The dielectric can be a free standing organic film, such as polyimide (Kapton, Upilex, etc.), a fiber (glass, aramide, etc., woven or non-woven) reinforced resin sheet, particulate filled fluoro-polymer liquid crystal film, or any of the other materials currently used as clad laminate materials in the PWB industry or base material in the flex circuit industry. The minimum requirements for the dielectric sheet/film are that it have sufficient mechanical integrity to support the conductive circuit features after they have been patterned, and that it not suffer detrimental effects at the required joining temperatures. After the minimums are met, complete freedom exists to optimize for other parameters such as electrical characteristics (dielectric constant and loss), mechanical properties, thermal properties, dimensional stability, etc. The conductive layer can be anything that can be patterned, and is solderable or can have a solderable surface layer applied. Metals, particularly copper, are especially suited. The conductive layer can be applied to the dielectric by laminating a foil, physical vapor deposition (vacuum evaporation or sputtering), plating (electro or electroless), chemical vapor deposition, or other means. Alternatively, the dielectric could be applied to a metal foil by such methods as screening, slot coating, curtain coating, doctor blading, roll coating, rod coating, spraying, etc. Two particularly advantageous classes of starting materials are: double sided, copper clad laminates, as commonly supplied to the PWB industry, and copper clad films, as commonly supplied to the flex circuit industry. A double sided, copper clad laminate has the advantage of having a rough, high area, surface, which will eventually need to bond with the infused liquid resin, after etching the laminated foil.

Step 1: (Optional - may not be needed for all process variations) Apply a removable protective coating (such as photo resist) over the metal clad side on which the circuit pattern is to be formed. This coating will allow etching the metal from the second side in the case of double sided clad starting material, protect the metal cladding from handling damage prior to circuit patterning, and act as a plating resist if dielectric via holes are to be filled with conductive material by a plating process. See Figure 2.

Step 2: (Optional - may not be needed for all process variations) Etch the metal cladding from the non-circuit side of a double sided clad starting material. See Figure 3.

Step 3: Form the via holes in the dielectric. This is best accomplished by laser drilling. However, it may be possible to adapt other processes, such as plasma etching, for this step at the cost of additional process complexity. See Figure 4.

Step 4: Fill the via holes in the dielectric with conductive material. The surface of the conductive fill should be even with, or slightly above the surface of the dielectric after via filling to assure good contact during joining. Fill can be accomplished by plating metal (either electroplating or electroless plating), or by forcing (e.g. by squeegeeing) conductive paste into the vias and curing. Having a continuous conductive layer on the circuit side of the layer is particularly advantageous in the case of electroplating. In the case of conductive paste via fill, it may be necessary to modify the surface of the fill material to assure good solder bonding during joining. See Figure 5.

Step 5: Cover the exposed surface of the via fill material with a thin (approximately 0.0001" - 0.0004") layer of tin or tin containing solder alloy. See Figure 6. This can be done with electroplating (in which case the continuous conductive layer on the circuit side is particularly advantageous) or electroless plating, both of which are maskless and self aligning for this process. Other solder alloys which are found to be compatible with fluxless soldering subsequent to a fluorine plasma treatment would be suitable replacements for tin containing solder alloys in these processes and structures.

Step 6: (Optional - may not be needed for all process variations) Remove any protective coating applied on the circuit side of the layer that was applied in Step 1.

Step 7: Apply, expose and develop a photo resist in the pattern of the circuitry desired on the metal clad side of the layer. See Figure 7.

Step 8: Etch the metal cladding into the desired circuit pattern, and remove the photo resist. See Figure 8.

Step 9: (Optional) Treat the layers with a immersion tin plating solution. This may enhance wetting, and thus yields, at joining, and the formation of a tin oxide on the surface of the copper circuitry may provide better adhesion of the infused resin to the circuitry than the native copper oxide.

Step 10: Treat the circuitized, via filled, layers in a fluorine containing plasma in accordance with US 4,921,157, 5,407,121 and/or 5,778,551. This is the key to obtaining metal surfaces (tin, solder, and/or copper) that can be soldered without the use of a soldering flux.

Step 11: Stack and align all of the component layers for the structure in the proper sequence. See Figure 9. For many applications, standard alignment methods, such as slots over pins, will provide adequate registration. For very dense structures with critical registration tolerances, optical alignment of adjacent layer pairs may be required. In either case, it is possible to reduce alignment shifts during mass joining by tack soldering a few joints per square inch as each new layer is added to the stack. Tack soldering can be accomplished by simply pressing over the joint location with a hot probe (fine tipped soldering iron) from the circuit side of the layer (for better heat transfer).

Step 12: Mass joining of the multi-layer structure by heating above the melting point of the solder which caps the filled vias. See Figure 10. Heating can be performed in a batch or conveyorized oven, or between heated platens. Light pressure, applied by parallel plates above and below the stack, is all that is needed to provide joint contact for joining. Pressure beyond that required to insure contact of surfaces to be joined is not needed or desirable. A traditional laminating press is not required. Joining atmosphere can be ambient, inert (e.g. nitrogen), or vacuum. Application of a vacuum at some point while at joining temperatures may improve the escape of any materials volatilized during the joining

process.

Step 13: Vacuum infuse a low viscosity, thermosetting resin into the open spaces between the joined layers. This can be achieved by a process known as vacuum bagging. A gas impermeable, flexible covering is placed around the structure, and sealed around the top and bottom periphery of the structure. A series of (generally opposed) vacuum and resin supply ports are placed around the edges of the joined structure. Surface tension and atmospheric pressure pushing on the resin supply cause the resin to flow into all of the open areas. The resin is then thermally cured, resulting in a monolithic structure. See Figure 11.

Production of the individual layers in the above disclosed process can be readily adapted to both panel processing and roll processing manufacturing tool sets.

MultiLam 2.PRZ Figures are contained in the attached Lotus Freelance presentation file (couldn't figure out how to

3. If the same advantage or problem has been identified by others (inside/outside IBM), how have those others solved it and does your solution differ and why is it better?

A practical, cost effective, method for parallel joining of multi-layer, organic dielectric, interconnect structures has long been sought by the electronics industry. All of the previously proposed solutions to this problem suffer from one or more major deficiencies, which has prevented their widespread adoption by the industry. The presently disclosed process does not suffer from the problems related below.

Gold Bonding

Thermo compression bonding of gold clad surfaces can provide a highly reliable metallurgical bond, but the joining process requires high temperatures and pressures, which limit the choice of materials for construction. Joining yields are negatively impacted by factors such as surface cleanliness and ability to provide uniform pressure to all of the different joint positions to be bonded. Also, the use of gold greatly increases the cost of this method.

Conductive Paste Bonding

The most common conductive pastes consist of conductive particles or flakes in a resin binder. These pastes depend on particle to particle, and particle to circuit feature, contact to maintain electrical conductivity. There are no metallurgical bonds holding the joint together. Reliable operation over the product lifetime requires that the conductive paste portion of each joint be maintained in compression, so that good particle contact is also maintained. Fabricating circuit layers, and/or bonding plies, to assure high joining yield (paste "slugs" must be crowned or dielectric must shrink in the out of plane direction during joining) while conforming to other process or product constraints (such as layer registration tolerance and dimensional stability, low out of plane expansion in the plane of the joints, adequate surface cleanliness for good joint conductivity, etc.) is difficult, resulting in low yields and/or high costs. Since there is no metallurgical bond with the circuit features, the interfaces may be susceptible to oxidation, and also corrosion if there is a diffusion path for moisture to the interfaces. Totally excluding moisture is extremely difficult in organic structures.

Newer conductive pastes, which do provide metallurgical bonds in the joints, are under development by

a number of companies. In these pastes the conductive particles are typically a solid solder alloy or coated with a solder alloy (Sn, Sn/Pb, Sn/Bi, etc.). At sufficiently high temperature (typically less than 240°C) the particles will metallurgically join to each other as well as the circuit features to be joined. The resin binders for these materials are typically thermosetting polymers that are designed to cure at about the same temperature as required for the metallurgical bonding. Two problems are associated with these types of conductive pastes. First, many such pastes require an extremely rapid heat up profile during joining, in order to allow proper metallurgical joining before the thermosetting resin becomes too rigid. It is extremely difficult to obtain the necessary heating rates throughout a multi-layer structure. Second, wetting and bonding to the surface of the circuit features requires a flux to remove oxides from the surface of the circuit features and the conductive particles. This effectively requires that the flux be a part of the paste binder system. The action of the flux when it chemically reduces the surface oxides also results in gases that must be eliminated from the structure, which can cause voiding or foaming of the paste binder. Also, all fluxes leave residues, which cannot be cleaned, due to the nature of the structures (large planes with very small gaps). Effective fluxes that provide benign residues for this type of application are yet to be developed. These newer pastes still have the requirement to provide some type of crowning or out of plane shrinkage in order to assure adequate contact for good joining yields.

4. If the invention is implemented in a product or prototype, include technical details, purpose, disclosure details to others and the date of that implementation.
na

***Critical Questions (Questions 1 - 7 must be answered)**

***Question 1** On what date was the invention workable? **Please format the date as MM-DD-YYYY** (Workable means i.e. when you know that your design will solve the problem)	
***Question 2** Is there any planned or actual publication or disclosure of your invention to anyone outside IBM?	○ Yes ● No
If yes, Enter the name of each publication or patent and the date published below. Publication/Patent: Date Published or Issued:	
Are you aware of any publications, products or patents that relate to this invention?	○ Yes ● No
If yes, Enter the name of each publication or patent and the date published below. Publication/Patent: Date Published or Issued:	

***Question 3** Has the subject matter of the invention or a product incorporating the invention been sold, used internally in manufacturing, announced for sale, or included in a proposal?	○ Yes ● No
Is a sale, use in manufacturing, product announcement, or proposal planned?	○ Yes ● No

If Yes, identify the product if known and indicate the date or planned date of sale, announcements, or proposal and to whom the sale, announcement or proposal has been or will be made.

Product:
Version/Release:
Code Name:
Date:
To Whom:

If more than one, use cut and paste and append as necessary in the field provided.

*Question 4	○ Yes ● No
Was the subject matter of your invention or a product incorporating your invention used in public, e.g., outside IBM or in the presence of non-IBMers?	
If yes, give a date. **Please format the date as MM-DD-YYYY**	

*Question 5	○ Yes ● No
Have you ever discussed your invention with others not employed at IBM?	
If yes, identify individuals and date discussed. Fill in the text area with the following information, the names of the individuals, the employer, date discussed, under CDA, and CDA #.	

*Question 6	○ Yes ● No ○ Not sure
Was the invention, in any way, started or developed under a government contract or project?	
If Yes, enter the contract number	

*Question 7	○ Yes ● No ○ Not Sure
Was the invention made in the course of any alliance, joint development or other contract activities?	
If Yes, enter the following :Name of Alliance, Contractor or Joint Developer	
Contract ID number	
Relationship contact name	
Relationship contact E-mail	
Relationship contact phone	

Question 8	○ Yes ● No
Have you submitted, or are you aware of, any related disclosure submission?	
If Yes, please provide the title and docket or disclosure number below:	

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Organic Dielectric Electronic Interconnect Structures and Method for Making

Question 9

What type of companies do you expect to compete with inventions of this type? *Check all that apply.*

- ☒ Manufacturers of enterprise servers
- ☒ Manufacturers of entry servers
- ☒ Manufacturers of workstations
- ☒ Manufacturers of PC's
- ☒ Non-computer manufacturers
- ☐ Developers of operating systems
- ☐ Developers of networking software
- ☐ Developers of application software
- ☐ Integrated solution providers
- ☐ Service providers
- ☒ Other (Please specify below)

Semiconductor packaging manufacturers, Electronic interconnect manufacturers

Patent Value Tool (Optional - this may be used by the inventor and attorney to assist with the eval

(The Patent Value tool can be used by you or the evaluation team to determine the potential licensing value of your invention.)

The **Patent Value Tool** has not yet been used to calculate a score.

Post Disclosure Text & Drawings

Enter any additional information relating to this disclosure below:

(Form Revised 12/17/97)